REMARKS

Pending in the application are claims 1-24, of which claims 1, 2, 8, 17 and 18 are independent. Claims 3, 18 and 24 have been amended to fix minor typographical errors. No new matter has been added. The following comments address all stated grounds for rejection and place the presently pending claims, as identified above, in condition for allowance

Amendments to the Claims

The Examiner has objected to Claim 18 because of an informality. Claim 18 has been amended to change "a advancing mechanism" to "an advancing mechanism" as suggested by the Examiner.

Claim 3 has been amended to add a period at the end of the claim.

Claim 24 has been amended to capitalize "An" at the beginning of the claim.

Rejection Pursuant to 35 U.S.C. §102(B)

The Examiner rejected claims 1-24 pursuant to 35 U.S.C. §102 (b) as being unpatentable over U.S. Patent No. 6,098,165 (hereinafter "Panwar"). Applicant respectfully traverses this rejection in light of the following arguments.

Summary of Claimed Invention

The claimed invention relates to the calculating of the number of valid instructions within a microprocessor instruction bundle. The calculation of the number of these valid instructions can be determined using edge detection techniques. Furthermore, the instructions within the bundle may be monotonically arranged, namely arranged in a manner wherein the order of the instructions are preserved. Furthermore, if dealing with instructions that are not monotonically arranged, the present invention can shift valid instructions to the top of the instruction bundle such that the valid instructions now lie onward from the first instruction slot

within the bundle. Using such an arrangement, upon encountering an invalid instruction before a valid instruction, the invalid instruction will be considered valid, but will be marked "not executable." Using such an arrangement, only instructions after the last valid instruction within the bundle will be invalid. The number of valid instructions within the bundle may now be determined using the faster and simpler method of edge detection.

Summary of Panwar

Panwar discloses a method of processing complex and non-complex instructions without penalizing the processing of non-complex instructions. In effectuating this goal, initially makes complete instructions with a marker bit, and allows these instructions to bypass the existing instruction pipeline such that the pipeline used by non-complex instructions. A controller is used to scan the marked instructions in the main bundle, and break up the main bundle of instructions into a smaller bundle that contains only complex instructions. The non-complex instructions are then processed in a manner in which they bypass the helper logic of Panwar, while complex instructions are processed and expanded into microinstructions using the helper logic. Using such an arrangement, the core non-complex instructions are not burdened by the presence of multiple complex instructions in a wide-issue processor.

Claim 1

Panwar fails to disclose each and every element of Claim 1. Panwar is directed to the handling of complex instructions in an instruction pipeline. Panwar does not disclose edge detecting valid instructions within the microprocessor as set forth in Claim 1. The Examiner appears to suggest that because the system of Panwar is clocked, Panwar discloses edge detecting valid instructions. This is not the case. Determining a clock cycle (which may be performed using edge detection) is not the same as determining the number of valid instructions. While the system of Panwar may be clocked, edge detection is not disclosed or even suggested as a method determining the number of valid instructions.

Furthermore, Panwar does not disclose a method for calculating the number of valid instructions within a microprocessor. The sections of Panwar cited by the Examiner (element

710 in Figure 7) refer to a valid vector indicating valid instructions in a sub-bundle. There is no discussion whatsoever of *a method for calculating* the number of valid instructions within the microprocessor.

In light of this, Applicants submit that the Panwar patent fails to disclose each element of Claim 1, and therefore ask the Examiner to withdraw the rejections to Claim 1 under 35 U.S.C. §102(B).

Claim 2

Panwar fails to disclose each and every element of Claim 2. Panwar is directed to the handling of complex instructions in an instruction pipeline. Panwar does not disclose edge detecting valid instructions within the bundle of instructions as set forth in Claim 2. The Examiner appears to suggest that because the system of Panwar is clocked, Panwar discloses edge detecting valid instructions. This is not the case. Determining a clock cycle (which may be performed using edge detection) is not the same as determining the number of valid instructions. While the system of Panwar may be clocked, edge detection is not disclosed or even suggested as a method determining the number of valid instructions.

In addition, Panwar does not disclose a method for calculating the number of valid instructions within a microprocessor. The sections of Panwar cited by the Examiner (element 710 in Figure 7) refer to a valid vector indicating valid instructions in a sub-bundle. There is no discussion whatsoever of *a method for calculating* the number of valid instructions within the microprocessor.

In light of this, Applicants submit that the Panwar patent fails to disclose each element of Claim 2, and therefore ask the Examiner to withdraw the rejections to Claim 2 under 35 U.S.C. §102(B).

Claims 3-7

Claims 3-7 depend from Claim 2 and as such incorporate each and every element of Claim 2. As set forth above, Panwar fails to disclose each and every element of Claim 2. Therefore Panwar does not disclose each and every element of claims 3-7.

In light of this, Applicants submit that the Panwar patent fails to disclose each element of Claims 3-7, and therefore ask the Examiner to withdraw the rejections to Claims 3-7 under 35 U.S.C. §102(B).

Claim 8

Panwar fails to disclose each and every element of Claim 8. As discussed above, Panwar is directed to the handling of complex instructions in an instruction pipeline. As with Claims 1 and 2, the Examiner appears to suggest that because the system of Panwar is clocked, Panwar discloses edge detecting valid instructions. Again, this is not the case. Determining a clock cycle (which may be performed using edge detection) is not the same as determining the number of valid instructions. While the system of Panwar may be clocked, edge detection is not disclosed or even suggested as a method determining the number of valid instructions. As such, Panwar does not disclose edge detecting valid instructions occurring after a complex instruction as set forth in Claim 8.

As stated before, Panwar discloses no methodology whatsoever for calculating the number of valid instructions. The sections of Panwar cited by the Examiner (element 710 in Figure 7) refer to a valid vector indicating valid instructions in a sub-bundle. There is no discussion whatsoever of *a method for calculating* the number of valid instructions within the microprocessor.

In light of this, Applicants submit that the Panwar patent fails to disclose each element of Claim 8, and therefore ask the Examiner to withdraw the rejections to Claim 8 under 35 U.S.C. §102(B).

Claims 9-16

Claims 9-16 depend from Claim 8 and as such incorporate each and every element of Claim 8. As set forth above, Panwar fails to disclose each and every element of Claim 8. Therefore Panwar does not disclose each and every element of claims 9-16.

In light of this, Applicants submit that the Panwar patent fails to disclose each element of Claims 9-16, and therefore ask the Examiner to withdraw the rejections to Claims 9-16 under 35 U.S.C. §102(B).

Claim 17

Panwar fails to disclose each and every element of Claim 17. Specifically, Panwar fails to disclose edge detecting valid instructions occurring after a complex instruction. As with Claims 1, 2, and 8 the Examiner appears to suggest that because the system of Panwar is clocked, Panwar discloses edge detecting valid instructions. Again, this is not the case. Determining a clock cycle (which may be performed using edge detection) is not the same as determining the number of valid instructions. While the system of Panwar may be clocked, edge detection is not disclosed or even suggested as a method determining the number of valid instructions.

As stated before, Panwar discloses no methodology whatsoever for calculating the number of valid instructions. As discussed above, Panwar is directed to the handling of complex instructions in an instruction pipeline. The sections of Panwar cited by the Examiner (element 710 in Figure 7) refer to a valid vector indicating valid instructions in a sub-bundle. There is no discussion whatsoever of *a method for calculating* the number of valid instructions within the microprocessor.

In light of this, Applicants submit that the Panwar patent fails to disclose each element of Claim 17, and therefore ask the Examiner to withdraw the rejections to Claim 17 under 35 U.S.C. §102(B).

Claim 18

Panwar fails to disclose each and every element of Claim 18. Specifically, Panwar fails to disclose an edge detecting element for detecting valid instructions within a bundle. As discussed above, Panwar is directed to the handling of complex instructions in an instruction pipeline. The sections of Panwar cited by the Examiner (element 710 in Figure 7) refer to a valid vector indicating valid instructions in a sub-bundle. The Examiner appears to suggest that because the system of Panwar is clocked Panwar discloses edge detecting valid instructions. Again, this is not the case. Nowhere in Panwar is there a discloser of an edge detection element *for detecting valid instructions within the bundle.* Determining a clock cycle (which may be performed using edge detection) is not the same as determining the number of valid instructions.

In light of this, Applicants submit that the Panwar patent fails to disclose each element of Claim 18, and therefore ask the Examiner to withdraw the rejections to Claim 18 under 35 U.S.C. §102(B).

Claims 19-24

Claims 19-24 depend from Claim 18 and as such incorporate each and every element of Claim 18. As set forth above, Panwar fails to disclose each and every element of Claim 18. Therefore Panwar does not disclose each and every element of claims 19-24.

In light of this, Applicants submit that the Panwar patent fails to disclose each element of Claims 19-24, and therefore ask the Examiner to withdraw the rejections to Claims 19-24 under 35 U.S.C. §102(B).

Conclusion

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 12-0080, under Order No. SMQ-143 (P6594) from which the undersigned is authorized to draw.

Dated: December 12, 2005

Respectfully submitted,

By _____

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